What Is Claimed Is:

1. A reset circuit of a timing controller, comprising:

a transistor including an emitter connected to a first node, a base connected to a second node and a collector connected to a third node, a digital input voltage (DVCC) being applied to the first node;

a first resistor connected between the first and second nodes;

a second resistor connected between the second node and a fourth node, the fourth node being grounded;

a third resistor connected between the third and fourth nodes;

a fourth resistor connected between the third node and a fifth node, the fifth node being connected to an input terminal of the timing controller; and

a capacitor including a first electrode connected to the fifth node and a second electrode that is grounded.

2. The circuit according to claim 1, wherein the transistor is a PNP (positive-negative-positive) type.

3. The circuit according to claim 1, wherein a ratio of the first resistor to the second and third resistors is substantially 100:51:1.

4. A circuit for a liquid crystal display device, comprising:

a timing controller including at least one input terminal;

a reset circuit connected to the timing controller, comprising:

a transistor including an emitter connected to a first node, a base connected to a second node and a collector connected to a third node, and a digital input voltage (DVCC) being applied to the first node;

a first resistor connected between the first and second nodes;

a second resistor connected between the second node and a fourth node, the fourth node being grounded;

a third resistor connected between the third and fourth nodes;

a fourth resistor connected between the third node and a fifth node, the fifth node being connected to the at least one input terminal; and

a capacitor including a first electrode connected to the fifth node and a second electrode grounded; and

a filtering circuit connected to the reset circuit, the filtering circuit permitting a gate operation enable (GOE) mask time of a GOE signal applied to a gate driver of the liquid crystal display device to be longer than about 16 msec and reducing an impulse of a clock signal applied to a source driver of the liquid crystal display device.

5. The circuit according to claim 4, wherein the transistor is a PNP (positive-negative-positive) type.

6. The circuit according to claim 4, wherein a ratio of the first resistor to the second and third resistors is substantially 100:51:1.

7. A liquid crystal display device, comprising:

an LCD module including a gate driver and a source driver;

a timing controller supplying a gate operation enable (GOE) signal to the gate driver and a clock signal to the source driver, the timing controller including an electrostatic protection circuit;

a reset circuit supplying a reset signal to the timing controller, the reset signal enabling the GOE signal; and

a filtering circuit connected to the reset circuit, the filtering circuit permitting a GOE mask time of the GOE signal to be longer than about 16 msec and reducing an impulse of the clock signal.

8. The device according to claim 7, wherein a digital input voltage (DVCC) is applied to the electrostatic protection circuit and the filtering circuit.

9. The device according to claim 8, wherein the filtering circuit includes first, second and third resistors and a transistor.

10. The device according to claim 9, wherein the transistor is a bipolar transistor including an emitter, a base and a collector.

11. The device according to claim 10, wherein a first end of the first resistor is connected to the emitter, a second end of the first resistor and a first end of the second resistor are connected to the base, a first end of the third resistor is connected to the collector, a second end of the second resistor and a second end of the third resistor are grounded, and the DVCC is applied to the emitter.

12. The circuit according to claim 11, wherein a ratio of the first resistor to the second and third resistors is substantially 100:51:1.

13. The device according to claim 12, wherein the reset circuit includes a fourth resistor and a capacitor having first and second electrodes.

14. The device according to claim 13, wherein a first end of the fourth resistor is connected to the collector, a second end of the fourth resistor is connected to the

first electrode of the capacitor and the timing controller, and the second electrode of the capacitor is grounded.

15. The device according to claim 8, wherein the DVCC has a first voltage of about 0.3 V to about 0.7V when an external main power is not applied to the timing controller and a second voltage of about 3.3 V when the external main power is applied to the timing controller.

16. A circuit for a liquid crystal display device, comprising:

a time controlling unit to supply an operation signal to a first driver of the liquid crystal display device and a timing signal to a second driver of the liquid crystal display device;

a resetting unit to supply an additional signal to the timing controller to enable the operation signal; and

a filtering unit to permit a masking of the operation signal for a time duration compatible with inducing a first driver operation involving substantially reduced image interferences, and to reduce an impulse of the timing signal.

17. The circuit according to claim 16, wherein the time duration of the masking of the operational signal is longer than about 16 msec.

18. A method of increasing reliability in a liquid crystal display device, the method comprising:

supplying an operation signal to a first driver of the liquid crystal display device and a timing signal to a second driver of the liquid crystal display device;

supplying an additional signal to a controller to enable the operation signal; and

filtering the additional signal to permit a masking of the operation signal for a time duration compatible with inducing a first driver operation involving substantially reduced image interferences, and to reduce an impulse of the timing signal.

19. The method as in claim 18, wherein the time duration of the masking of the operational signal is longer than about 16 msec.